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DESIGN AND DEVELOPMENT OF HARDWARE AND FIRMWARE FOR A MULTIFUNCTIONAL SMD FREQUENCY SYNTHESIZER

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Abstract: The aim of this project is to design and develop hardware and firmware that are required for a multifunctional surface mount frequency synthesizer. The applications of this design includes following:
a) Remote sensing Data down convertor
b) QPSK Modulation

In Remote sensing data down convertor the frequency synthesizer, plays the important role of Local Oscillator carrier generation for mixing with the RF signal to generate fixed IF frequency. In the design of QPSK modulator it is used to provide variable clocks required by the FPGA to cater to the various data rates and also as the carrier signal. This development is centered around the design of SMD frequency synthesizer with Phase locked loop Logic.LMX 2541 ultralow noise frequency synthesizer is used here and it is initialized and configured for operation using AT89C55WD microcontroller unit. The firmware developed also includes handling peripheral devices like keypad and LCD display for configuration of the unit in stand-alone mode. The firmware was developed using Embedded C programming language on Keil platform.

Keywords: Remote sensing, frequency synthesizer, phase locked loop, KEIL

I.INTRODUCTION

The use of extremely sophisticated circuitry in the down converter leads to exorbitant costs and increases system complexity. By using surface mount frequency synthesizer we can reduce the cost and generates an improved down converter that can be used in satellite communication system.

In order to achieve the desired objectives the LMX2541 is used as a frequency synthesizer. LMX2541 eliminates need for bulky and expensive local oscillator modules. LMX2541 is well suited for local oscillator applications in the next generation base station radio transceivers. When paired with LMK04000 clock jitter cleaner, the LMX2541 significantly improves system error vector magnitude (EVM), resulting in enhanced receiver sensitivity and transmitter spectral purity. The proposed design for the down convertor eliminates the need for complex circuitry and it's cost effective.

II.FREQUENCY SYNTHESIZER

A frequency synthesizer is a device (an electronic system) that generates a large number of precise frequencies from a single reference frequency. A frequency synthesizer can replace the expensive array of crystal resonators in a multichannel radio receiver. A single-crystal oscillator provides a reference frequency, and the frequency synthesizer generates the other frequencies. Because they are relatively inexpensive and because they can be easily controlled by digital circuitry, frequency synthesizers are being included in many new communication system designs. frequency synthesizer can combine frequency multiplication, frequency division, and frequency mixing operations to produce the desired output signal There are two types of frequency synthesizers one is Direct frequency synthesizer and another is frequency synthesis by phase-locked loop. The Direct frequency synthesizer is the oldest of the frequency synthesis methods. It synthesizes a specified frequency from one or more reference frequencies from a combination of harmonic generators, band-pass filters, dividers, and frequency mixers. Highly selective filters are required with this method..The disadvantages associated with direct synthesis are greatly diminished with the frequency synthesis technique (often referred to as indirect synthesis) that employs a phase-locked loop. The PLL with a frequency divider in the loop thus provides a method for obtaining a large number of frequencies from a single reference frequency. If the divide ratio N is realized by using a programmable divider (integrated circuitry has made the digital programmable divider an inexpensive

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circuit component), it is possible to easily change the output frequency in increments

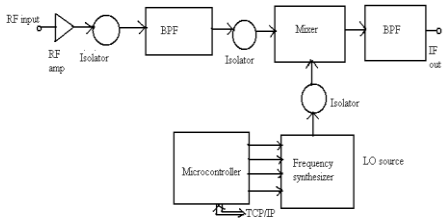

Fig 1: Block Diagram of data down convertor

In Remote sensing data down convertor the frequency synthesizer, plays the main role of carrier generation for the down-conversion in generating fixed IF frequency by eliminating the need of bulky local oscillators.

The design of the system is explained as follows.

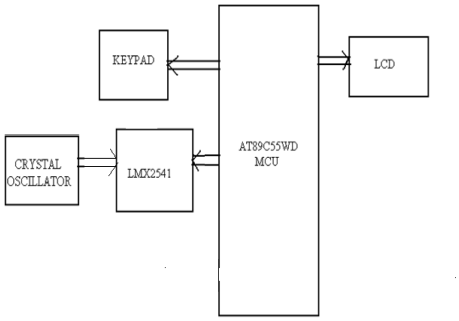

Fig 2: Block Diagram of system

Subsystem details can be explained as below:

Crystal oscillator:

A single-crystal oscillator provides a reference frequency. The frequency synthesizer board consists of 100MHz and 50MHz crystal oscillators.

LMX 2541:

The LMX2541 features a fully integrated, ultra-low noise delta sigma fractional-N PLL, voltage controlled oscillator (VCO), divider and output driver.

It consists of 36-Pin in NJK0036A Package

The PLL offers a normalized noise floor of -225dBc/Hz and can be operated up to104MHZ of phase detector rate (comparison frequency) in both integer and fractional modes. It also can be configured to work with an external VCO, fast lock mode with cycle-slip reduction and a low noise, integrated-input crystal oscillator circuit

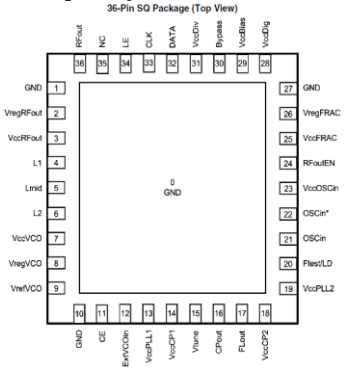

Fig 3: Pin Diagram of LMX 2541

In addition, the LMX2541 integrates the necessary low-dropout (LDO) regulators and output-driver matching network to provide higher supply noise immunity and more consistent performance, while reducing the number of external components. The LMX2541's supply voltage range is 3.15V to 3.45V and device programming is facilitated using a three-wire MICROWIRE bus interface that can operate down to 1.8V. The LMX2541 is a low power, high performance frequency synthesizer system which includes a PLL, Partially Integrated Loop Filter, VCO, VCO Divider, and Programmable Output Buffer. There are three basic modes that the device can be configured in: Full Chip Mode, External VCO Mode, and Divider Only Mode. Full chip mode is intended to be used with the internal VCO and PLL. There is also the option of External VCO mode, which allows the user to connect their own external VCO. Finally, there is Divider only, which is just the VCO divider and output buffer.

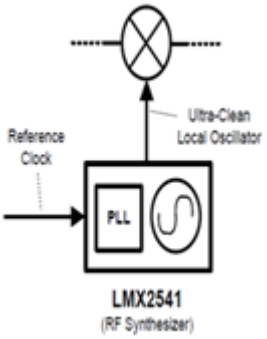

Fig 4: Block Diagram of LMX 2541

The frequency coverage range of LMX 2541 is as follows

Table 1: Frequency coverage of LMX2541

Device	VCO Frequency
LMX2541SQ2060E	1990 – 2240
LMX2541SQ2380E	2200 – 2530
LMX2541SQ2690E	2490 – 2865
LMX2541SQ3030E	2810 – 3230
LMX2541SQ3320E	3130 – 3600
LMX2541SQ3740E	3480 – 4000

All devices have continuous frequency coverage below a divide value of 8 (7 for most devices) down to their minimum frequency achievable with divide by 63.

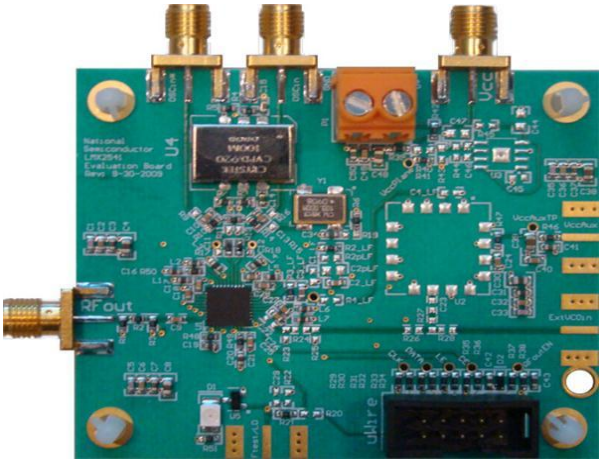

Fig 5: Evaluation Board of LMX 2541

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Keypad: The MM74C922N CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost Switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data available output goes to a high level when a valid keyboard entry has been made. The Data available output returns to a low level when the entered key is released, even if another key is depressed. The Data available will return high to indicate acceptance of the new key after a normal debounce period; this two-key rollover is provided between any two switches. An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

LCD: The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcontroller in the external RAM to generate dot matrix liquid crystal driving signals. It has a graphic mode in which 1-bit data in the external RAM corresponds to the on/off state of 1 dot on liquid crystal display and a character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications

AT89C55WD Microcontroller:

The AT89C55WD is a low-power; high-performance CMOS 8-bit microcontroller with 20K bytes of Flash programmable read only memory and 256 bytes of RAM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pin out. The on-chip Flash allows the program memory to be user programmed by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C55WD is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications. The AT89C55WD provides the following standard features: 20K bytes of flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer /counters, a six vector, two-level interrupt architecture, a full-duplex serial port, on-chip oscillator, and clock circuitry. In addition the AT89C55WD is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The ideal mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power down mode saves the RAM contents but freezes oscillator, disabling all other chip functions until the next external interrupt or hardware reset

The AMS1117 series of adjustable and fixed voltage regulators are designed to provide up to1A output current and to operate down to 1V input-to-output differential. The dropout voltage of the device is guaranteed maximum 1.3V, decreasing at lower load currents

III. PROGRAMMING LMX2541 USING AT89C55WD

The LMX2541 is programmed using several 32-bit registers used to control the LMX2541 operation. By changing the register values according to the desired frequency in the LMX2541, we will get the divider value, resistor and capacitor values. Here we can even select the power-down mode for low power requirements. A 32-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last 4 register bits, CTRL [3:0] form the address field, which is used to decode the internal register address. The remaining 28 bits form the data field DATA [27:0].

While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank. For initial device programming the register programming sequence must be done in the order of the register map. The action of programming register R7 and bringing LE low resets all the registers to default values, including hidden registers. The programming of register R0 is also special for the device when operating in full chip mode because the action of programming either one of these registers activates the VCO calibration.R0 lower, R1 upper, R4 lower are programmable registers and the values of remaining registers are obtained from CODE LOADER software and are constant

For example: if we require the output frequency as 2874 MHz then we will select the 3030E a family then the register values are calculated or can be generated by using the codeloder4 software and then loaded into the source code.

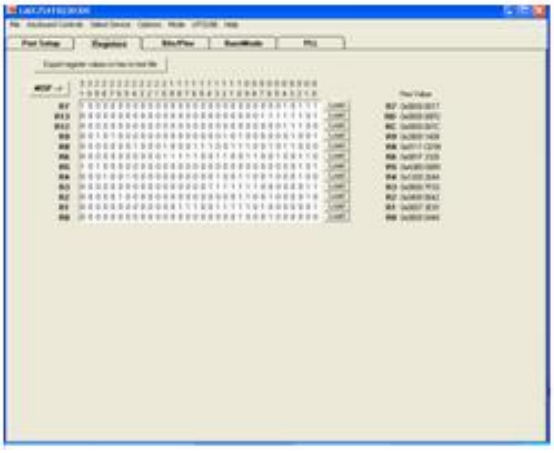

Fig 6: Register values on Code loader software

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SERIAL DATA TIMING DIAGRAM

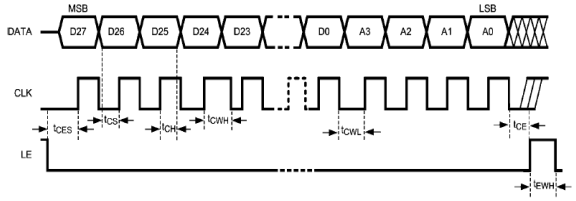

Fig 7: Serial data timing Diagram

The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter. After the programming is complete, the CLK, DATA, and LE signals should be returned to a low state. If the CLK and DATA lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

Softwares :

The software used in the project are:

Keil software for C programming

TI clock design tool

TI clock design:

TI Clock Design Tool software is used to aid part selection, loop filter design, and simulation of timing device solutions. Enter desired output frequencies and optionally a reference frequency and the tool provides, divider values, and recommended loop filter to minimize jitter.It also gives R, C values required in the design of PLL.

The primary purpose of National's Clock Design Tool is to:
a) Aid the user in selecting a National Timing device as their clocking solution.
b) Aid the user in designing a loop filter for optimum phase noise/jitter for their selected solution. . Blocks of PLL such as the Phase detector, frequency detector when driven, the transition at their output is a direct result of a transition at their input. The jitter exhibited by these blocks is referred to as synchronous jitter, it is a variation in the delay between when the input is received and the output is produced. Blocks such as the OSC and VCO are autonomous. They generate output transitions not as a result of transitions at their inputs, but rather as a result of the previous output transition. The jitter produced by these blocks is referred to as accumulating jitter Keilμvision3 is an IDE (integrated development environment) that helps you write, compile, and debug embedded programs. It is basically an assembler and a compiler. The μVision IDE from Keil combines project management, make facilities, source code editing, program debugging, and complete simulation in one powerful environment. The μVision development platform is easy- to-use and quickly creates embedded programs that work.

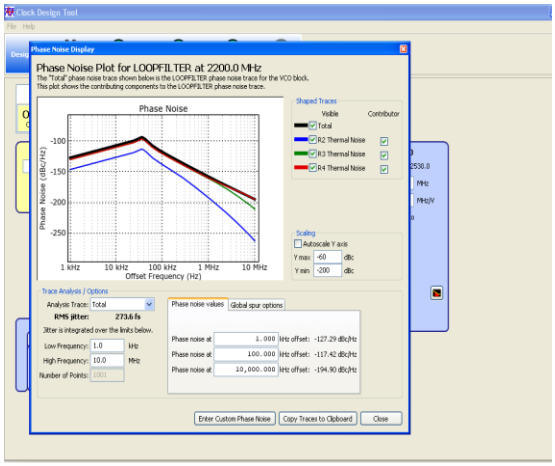

Fig 8: Output on clock design tool KEIL μVISION3

The μVision editor and debugger are integrated in a single application that provides a seamless embedded project development environment. When we use the Keil Software tools, the 8051 project development cycle is roughly the same as for any software development project. Programming in C makes the embedded systems more reliable. C code written for a specific micro controller can easily be transferred to systems using different micro controllers of different vendors without little or no modification. It can be reused, easy to maintain and easy to debug and extend.

EMBEDDED C

The programming language used here in this project is Embedded C language. This Embedded C language is different from general C language in few things It uses most of the syntax and semantics of standard C, such as main() function, variable definition, data type declaration, conditional statements (if, switch. case), loops (while, for), functions, arrays and strings, structures and union, bit operations, macros, unions, etc.

In order to support exotic features, the embedded C programming requires nonstandard extensions to the C language. These features include fixed-point arithmetic, multiple distinct memory banks, and basic I/O operations

IV.RESULTS

Output waveform observed on Spectrum Analyzer

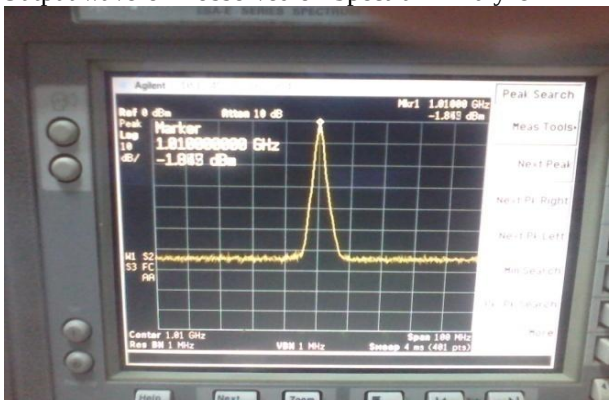

Fig 9: Output Waveform

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LCD display

Fig 10: LCD display

V.CONCLUSION

This project presents the design and implementation of hardware and firmware of surface mount frequency synthesizer which improves the phase noise performance significantly, besides providing flexibility and adaptability to suit various applications. It also proves to be a compact and cost-effective solution.

The design is implemented without using jitter cleaners thus reducing the components and complexity in design

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